

70-V Fault-Protected RS-485 Transceivers

FEATURES

- Bus-Pin Fault Protection to $> \pm 70$ V
- Common-Mode Voltage Range (-20 V to 25 V) More Than Doubles TIA/EIA 485 Requirement
- Bus I/O Protection
 - ± 16 kV JEDEC HBM Protection
- Reduced Unit Load for Up to 256 Nodes
- Failsafe Receiver for Open-Circuit, Short-Circuit and Idle-Bus Conditions

- Low Power Consumption
 - Low Standby Supply Current, 1 μ A Typ
 - I_{CC} 5 mA Quiescent During Operation
- Power-Up, Power-Down Glitch-Free Operation

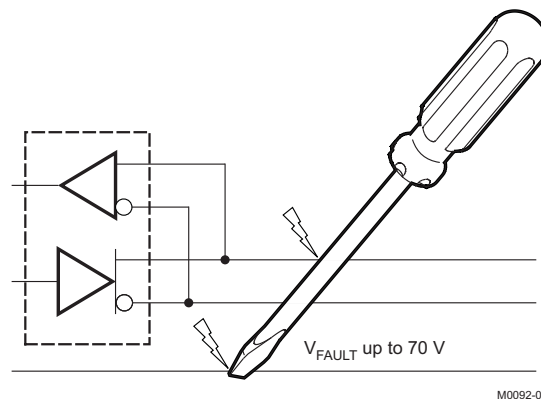
APPLICATIONS

- Designed for RS-485 and RS-422 Networks

DESCRIPTION

These devices are designed to survive overvoltage faults such as direct shorts to power supplies, mis-wiring faults, connector failures, cable crushes, and tool mis-applications. They are also robust to ESD events, with high levels of protection to human-body model specifications.

These devices combine a differential driver and a differential receiver, which operate from a single power supply. In the 'HVD1785, 'HVD1786, and 'HVD1787, the driver differential outputs and the receiver differential inputs are connected internally to form a bus port suitable for half-duplex (two-wire bus) communication. In the 'HVD1791, the driver differential outputs and the receiver differential inputs are separate pins, to form a bus port suitable for full-duplex (four-wire bus) communication. These ports feature a wide common-mode voltage range, making the devices suitable for multipoint applications over long cable runs. These devices are characterized from -40°C to 105°C .



M0092-01

PRODUCT SELECTION GUIDE

PART NUMBER	DUPLEX	SIGNALING RATE	NODES	CABLE LENGTH
SN65HVD1785	Half	115 kbps	Up to 256	1500 m
SN65HVD1786	Half	1 Mbps	Up to 256	150 m
SN65HVD1787	Half	10 Mbps	Up to 64	50 m
SN65HVD1791	Full	115 kbps	Up to 256	1500 m
SN65HVD1792 (Preview)	Full	1 Mbps	Up to 256	150 m
SN65HVD1793 (Preview)	Full	10 Mbps	Up to 64	50 m

For similar features with 3.3 V supply operation, see the SN65HVD1781 ([SLLS877](#)).

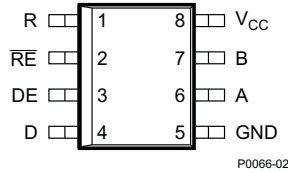


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



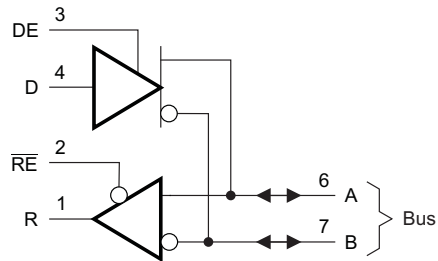
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

SN65HVD1785, 1786, 1787
 D or P Package
 (Top View)



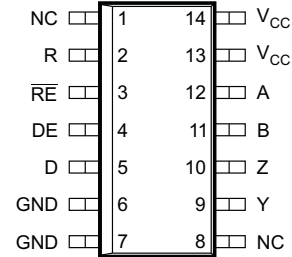
P0066-02

Logic Diagram (Positive Logic)



S0299-01

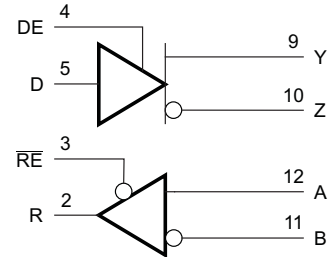
SN65HVD1791, 1792, 1793
 D Package
 (Top View)



NC - No internal connection

P0005-02

Logic Diagram (Positive Logic)



S0300-01

DEVICE INFORMATION

DRIVER FUNCTION TABLE

Input	Enable	Outputs		
		A	B	
H	H	H	L	Actively drive bus High
L	H	L	H	Actively drive bus Low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drive bus High by default

RECEIVER FUNCTION TABLE

Differential Input	Enable	Output	
$V_{ID} = V_A - V_B$	RE	R	
$V_{IT+} < V_{ID}$	L	H	Receive valid bus High
$V_{IT-} < V_{ID} < V_{IT+}$	L	?	Indeterminate bus state
$V_{ID} < V_{IT-}$	L	L	Receive valid bus Low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

	VALUE	UNIT
V_{CC} Supply voltage	–0.5 to 7	V
Voltage range at A and B inputs	–70 to 70	V
Input voltage range at any logic pin	–0.3 to $V_{CC} + 0.3$	V
Voltage input range, transient pulse, A and B, through 100 Ω	–100 to 100	V
Receiver output current	–24 to 24	mA
T_J Junction temperature	170	°C
Continuous total power dissipation	See Dissipation Rating Table	
IEC 60749-26 ESD (human-body model), bus terminals and GND	± 16	kV
JEDEC Standard 22, Test Method A114 (human-body model), bus terminals and GND	± 16	kV
JEDEC Standard 22, Test Method A114 (human-body model), all pins	± 4	kV
JEDEC Standard 22, Test Method C101 (charged-device model), all pins	± 2	kV
JEDEC Standard 22, Test Method A115 (machine model), all pins	± 400	V

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

PACKAGE DISSIPATION RATINGS

PACKAGE	JEDEC THERMAL MODEL	$T_A < 25^\circ\text{C}$ RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 85^\circ\text{C}$ RATING	$T_A = 105^\circ\text{C}$ RATING
SOIC (D) 8-pin	High-K	905 mW	7.25 mW/°C	470 mW	325 mW
	Low-K	516 mW	4.1 mW/°C	268 mW	186 mW
SOIC (D) 14-pin	High-K	1315 mW	10.5 mW/°C	684 mW	474 mW
	Low-K	744 mW	6 mW/°C	387 mW	268 mW
PDIP (P) 8-pin	High-K	2119 mW	16.9 mW/°C	1100 mW	763 mW
	Low-K	976 mW	7.8 mW/°C	508 mW	352 mW

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
V_{CC} Supply voltage	4.5	5	5.5	V
V_I Input voltage at any bus terminal (separately or common mode) ⁽¹⁾	–20		25	V
V_{IH} High-level input voltage (driver, driver enable, and receiver enable inputs)	2		V_{CC}	V
V_{IL} Low-level input voltage (driver, driver enable, and receiver enable inputs)	0		0.8	V
V_{ID} Differential input voltage	–25		25	V
I_O Output current	Output current, driver		60	mA
	Output current, receiver	–8	8	mA
R_L Differential load resistance	54	60		Ω
C_L Differential load capacitance		50		pF
$1/t_{UI}$ Signaling rate	HVD1785, HVD1791		115	kbps
	HVD1786, HVD1792		1	Mbps
	HVD1787, HVD1793		10	
T_A Operating free-air temperature (See application section for thermal information)	–40		105	°C
T_J Junction temperature	–40		150	°C

- (1) By convention, the least positive (most negative) limit is designated as minimum in this data sheet.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT		
V _{OD}	Driver differential output voltage magnitude	RS-485 with common-mode load, V _{CC} > 4.75 V, see Figure 1	T _A ≤ 85°C	1.5			V		
			T _A ≤ 105°C	1.4					
		R _L = 54 Ω, 4.75 V ≤ V _{CC} ≤ 5.25 V	1.5	2					
		R _L = 100 Ω, 4.75 V ≤ V _{CC} ≤ 5.25 V	2	2.5					
Δ V _{OD}	Change in magnitude of driver differential output voltage	R _L = 54 Ω		-0.2	0	0.2	V		
V _{OC(SS)}	Steady-state common-mode output voltage			1	V _{CC} /2	3	V		
ΔV _{OC}	Change in differential driver output common-mode voltage			-100	0	100	mV		
V _{OC(PP)}	Peak-to-peak driver common-mode output voltage	Center of two 27-Ω load resistors, See Figure 2			500		mV		
C _{OD}	Differential output capacitance				23		pF		
V _{IT+}	Positive-going receiver differential input voltage threshold	V _{CM} = -20 V to 25 V			-100	-10	mV		
V _{IT-}	Negative-going receiver differential input voltage threshold				-200	-150	mV		
V _{HYS}	Receiver differential input voltage threshold hysteresis (V _{IT+} - V _{IT-})				30	50	mV		
V _{OH}	Receiver high-level output voltage	I _{OH} = -8 mA		2.4	V _{CC} -0.3		V		
V _{OL}	Receiver low-level output voltage	I _{OL} = 8 mA	T _A ≤ 85°C		0.2	0.4	V		
			T _A ≤ 105°C		0.2	0.5			
I _I	Driver input, driver enable, and receiver enable input current			-100		100	μA		
I _{OZ}	Receiver output high-impedance current	V _O = 0 V or V _{CC} , RE at V _{CC}		-1		1	μA		
I _{OS}	Driver short-circuit output current			-250		250	mA		
I _I	Bus input current (disabled driver)	V _{CC} = 4.5 to 5.5 V or V _{CC} = 0 V, DE at 0 V	85, 86, 91, 92	V _I = 12 V		75	125	μA	
				V _I = -7 V	-100	-40			
			87, 93	V _I = 12 V			500		
				V _I = -7 V	-400				
I _{CC}	Supply current (quiescent)	Driver and receiver enabled	DE = V _{CC} , RE = GND, no load		4	6	mA		
			Driver enabled, receiver disabled	DE = V _{CC} , RE = V _{CC} , no load		3		5	
			Driver disabled, receiver enabled	DE = GND, RE = GND, no load		2		4	
			Driver and receiver disabled	DE = GND, D = open RE = V _{CC} , no load		0.5	5	μA	
Supply current (dynamic)		See TYPICAL CHARACTERISTICS section							

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
DRIVER (HVD1785 AND HVD1791)							
t_r, t_f	Driver differential output rise/fall time	$R_L = 54 \Omega, C_L = 50 \text{ pF}$, See Figure 3	0.4	1.7	2.6	μs	
t_{PHL}, t_{PLH}	Driver propagation delay			0.8	2	μs	
$t_{SK(P)}$	Driver differential output pulse skew, $ t_{PHL} - t_{PLH} $			20	250	ns	
t_{PHZ}, t_{PLZ}	Driver disable time			0.1	5	μs	
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled		0.2	3	μs	
		Receiver disabled		3	12		
DRIVER (HVD1786 AND HVD1792)							
t_r, t_f	Driver differential output rise/fall time	$R_L = 54 \Omega, C_L = 50 \text{ pF}$, See Figure 3		50	300	ns	
t_{PHL}, t_{PLH}	Driver propagation delay				200	ns	
$t_{SK(P)}$	Driver differential output pulse skew, $ t_{PHL} - t_{PLH} $				25	ns	
t_{PHZ}, t_{PLZ}	Driver disable time			3	μs		
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled			300	ns	
		Receiver disabled			10	μs	
DRIVER (HVD1787 AND HVD1793)							
t_r, t_f	Driver differential output rise/fall time	$R_L = 54 \Omega, C_L = 50 \text{ pF}$, See Figure 3	3		30	ns	
t_{PHL}, t_{PLH}	Driver propagation delay				50	ns	
$t_{SK(P)}$	Driver differential output pulse skew, $ t_{PHL} - t_{PLH} $				10	ns	
t_{PHZ}, t_{PLZ}	Driver disable time			3	μs		
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled			300	ns	
		Receiver disabled			9	μs	
RECEIVER (ALL DEVICES UNLESS OTHERWISE NOTED)							
t_r, t_f	Receiver output rise/fall time	$C_L = 15 \text{ pF}$, See Figure 6		4	15	ns	
t_{PHL}, t_{PLH}	Receiver propagation delay time		85, 86, 91, 92		100	200	ns
			87, 93			70	
$t_{SK(P)}$	Receiver output pulse skew, $ t_{PHL} - t_{PLH} $		85, 86, 91, 92		6	20	ns
		87, 93			5		
t_{PLZ}, t_{PHZ}	Receiver disable time	Driver enabled, See Figure 7		15	100	ns	
$t_{PZL(1)}, t_{PZH(1)}$ $t_{PZL(2)}, t_{PZH(2)}$	Receiver enable time	Driver enabled, See Figure 7		80	300	ns	
		Driver disabled, See Figure 8		3	9	μs	

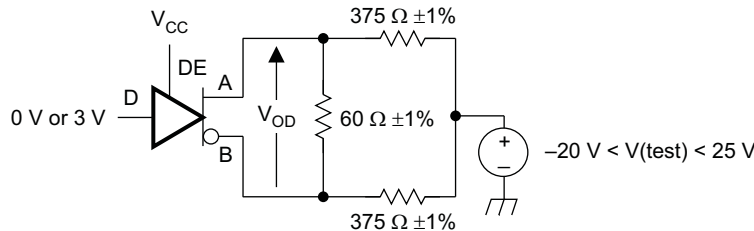
THERMAL INFORMATION

PARAMETER		TEST CONDITIONS	VALUE	UNIT	
R _{θJA}	Junction-to-ambient thermal resistance (no airflow)	SOIC-8	JEDEC high-K model	138	°C/W
			JEDIC low-K model	242	
		DIP-8	JEDEC high-K model	59	
			JEDIC low-K model	128	
		SOIC-14	JEDEC high-K model	95	
			JEDIC low-K model	168	
R _{θJB}	Junction-to-board thermal resistance	SOIC-8	62	°C/W	
		DIP-8	39		
		SOIC-14	40		
R _{θJC}	Junction-to-case thermal resistance	SOIC-8	61	°C/W	
		DIP-8	61		
		SOIC-14	44		
P _D	Power dissipation	85, 91	V _{CC} = 5.5 V, T _J = 150°C, R _L = 300 Ω, C _L = 50 pF (driver), C _L = 15 pF (receiver) 5-V supply, unterminated ⁽¹⁾	290	mW
		85, 91	V _{CC} = 5.5 V, T _J = 150°C, R _L = 100 Ω, C _L = 50 pF (driver), C _L = 15 pF (receiver) 5-V supply, RS-422 load ⁽¹⁾	320	
		86			
		87			
		85, 91	V _{CC} = 5.5 V, T _J = 150°C, R _L = 54 Ω, C _L = 50 pF (driver), C _L = 15 pF (receiver) 5-V supply, RS-485 load ⁽¹⁾	400	
		86			
87					
T _{SD}	Thermal-shutdown junction temperature		170	°C	

(1) Driver and receiver enabled, 50% duty cycle square-wave signal at signaling rate: HVD1785, 1791 at 115 kbps, HVD1786 at 1 Mbps, HVD1787 at 10 Mbps)

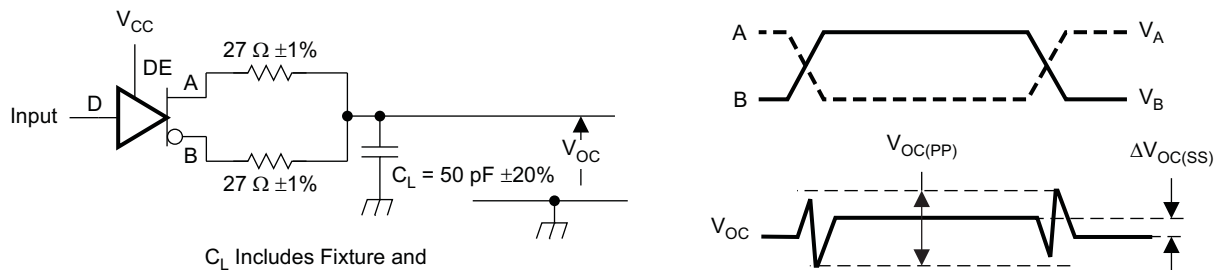
PARAMETER MEASUREMENT INFORMATION

Input generator rate is 100 kbps, 50% duty cycle, rise and fall times less than 6 nsec, output impedance 50 Ω.



S0301-01

Figure 1. Measurement of Driver Differential Output Voltage With Common-Mode Load



C_L Includes Fixture and Instrumentation Capacitance

S0302-01

Figure 2. Measurement of Driver Differential and Common-Mode Output With RS-485 Load

PARAMETER MEASUREMENT INFORMATION (continued)

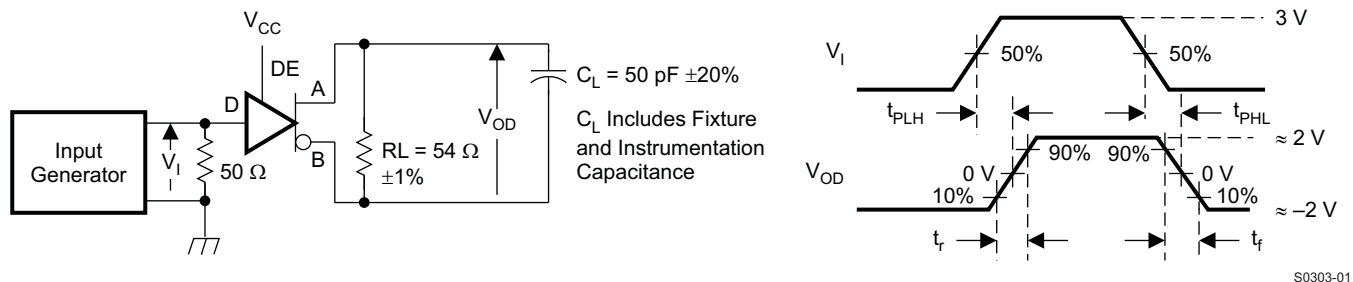
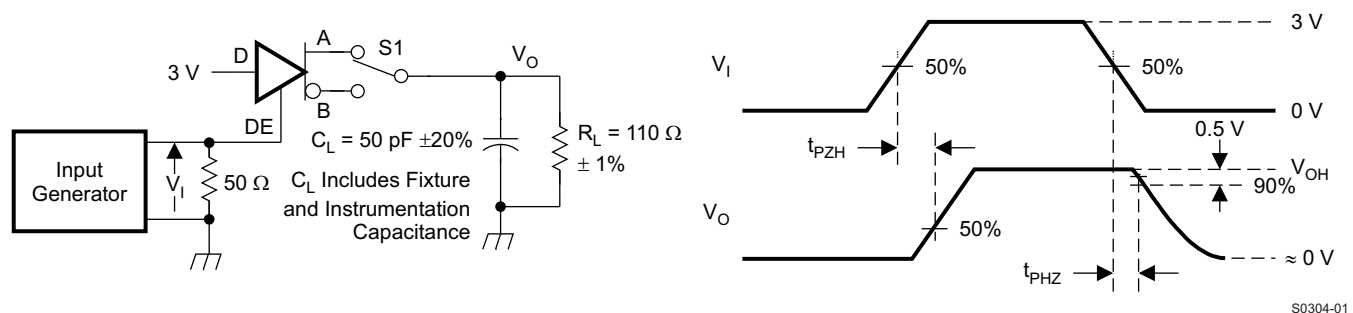
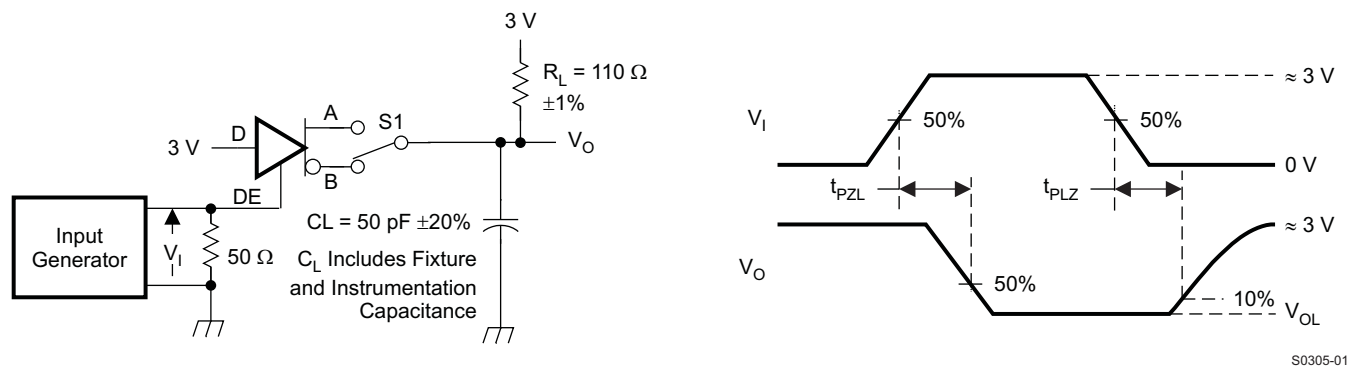


Figure 3. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays



NOTE: D at 3 V to test non-inverting output, D at 0 V to test inverting output.

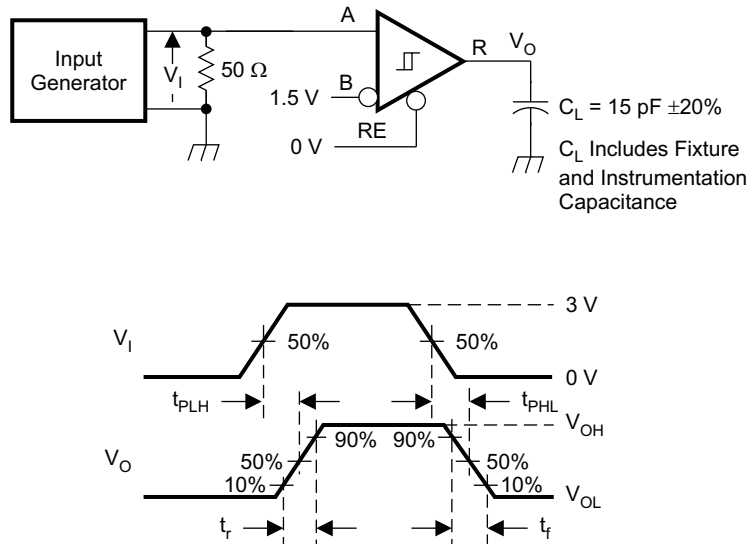
Figure 4. Measurement of Driver Enable and Disable Times With Active High Output and Pulldown Load



NOTE: D at 0 V to test non-inverting output, D at 3 V to test inverting output.

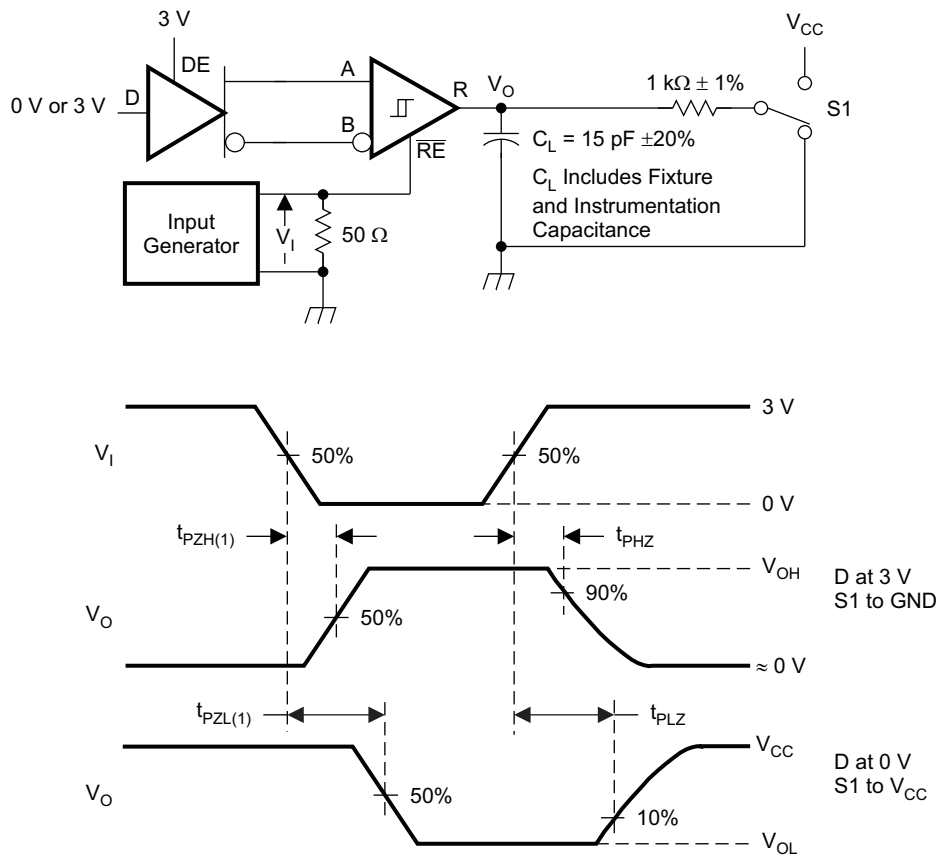
Figure 5. Measurement of Driver Enable and Disable Times With Active-Low Output and Pullup Load

PARAMETER MEASUREMENT INFORMATION (continued)



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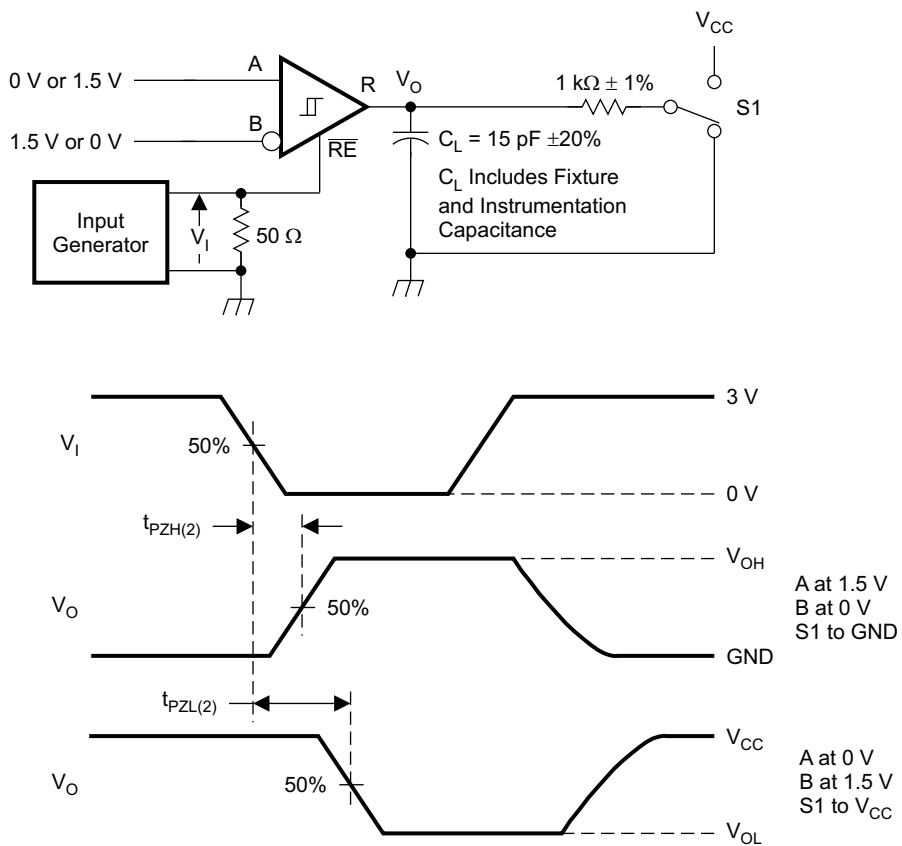
Figure 6. Measurement of Receiver Output Rise and Fall Times and Propagation Delays



S0307-01

Figure 7. Measurement of Receiver Enable/Disable Times With Driver Enabled

PARAMETER MEASUREMENT INFORMATION (continued)



S0308-01

Figure 8. Measurement of Receiver Enable Times With Driver Disabled

TYPICAL CHARACTERISTICS

DRIVER OUTPUT CURRENT
vs
SUPPLY VOLTAGE

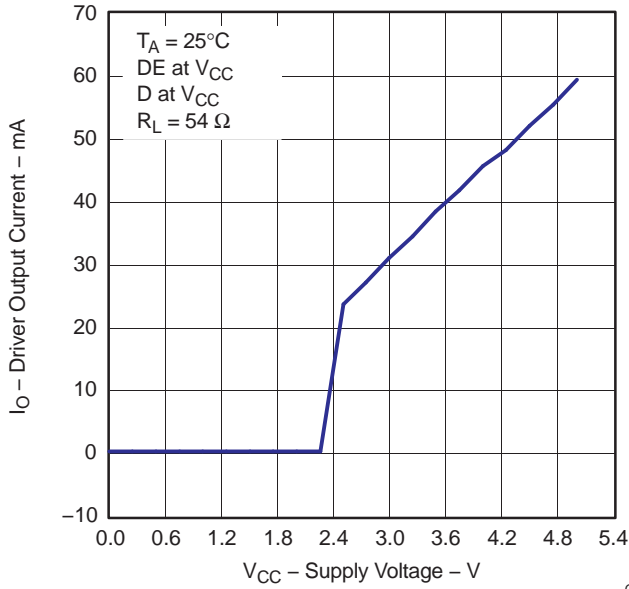


Figure 9.

G001

RMS SUPPLY CURRENT
vs
SIGNALING RATE

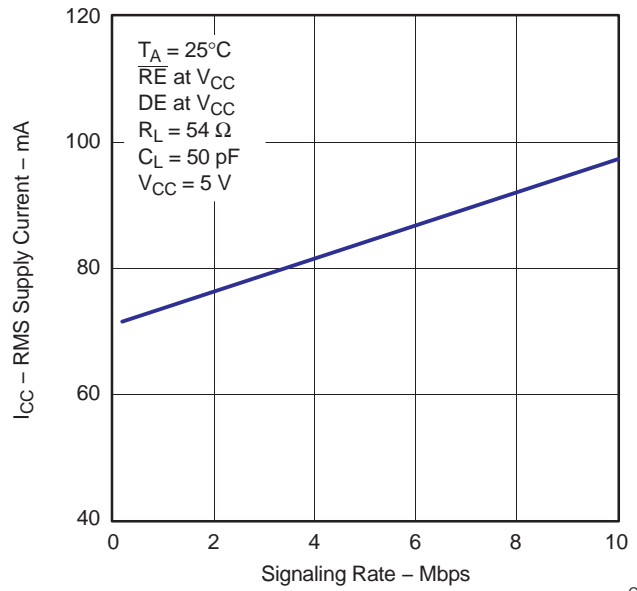


Figure 10.

G002

BUS PIN CURRENT
vs
BUS PIN VOLTAGE

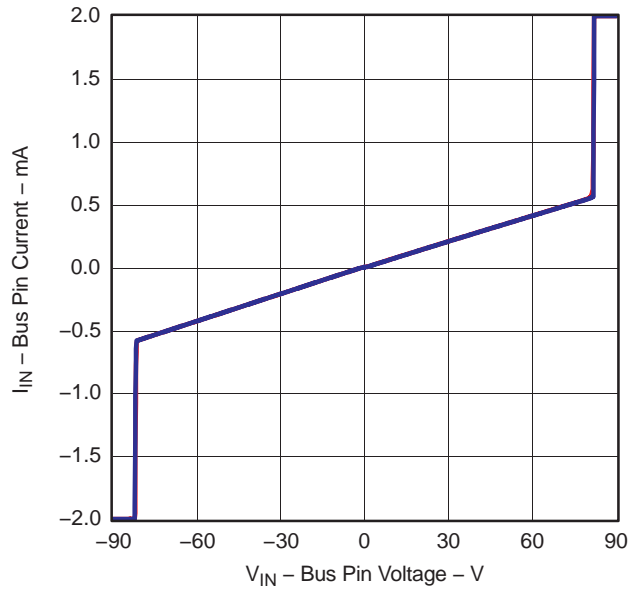


Figure 11.

G004

ADDITIONAL OPTIONS

The SN65HVD17xx family also has options for J1708 applications, for always-enabled full-duplex versions (industry-standard SN65LBC179 footprint) and for inverting-polarity versions, which allow users to correct a reversal of the bus wires without re-wiring. Contact your local Texas Instruments representative for information on these options.

PART NUMBER	SN65HVD17xx		
	SLOW	MEDIUM	FAST
Half-duplex (176 pinout)	85	86	87
Full-duplex no enables (179 pinout)	88	89	90
Full-duplex with enables (180 pinout)	91	92	93
Half-duplex with cable invert	94	95	96
Full-duplex with cable invert and enables	97	98	99
J1708	08	09	10



Figure 12. SN65HVD1708E Transceiver for J1708 Applications



Figure 13. SN65HVD17xx Always-Enabled Driver Receiver

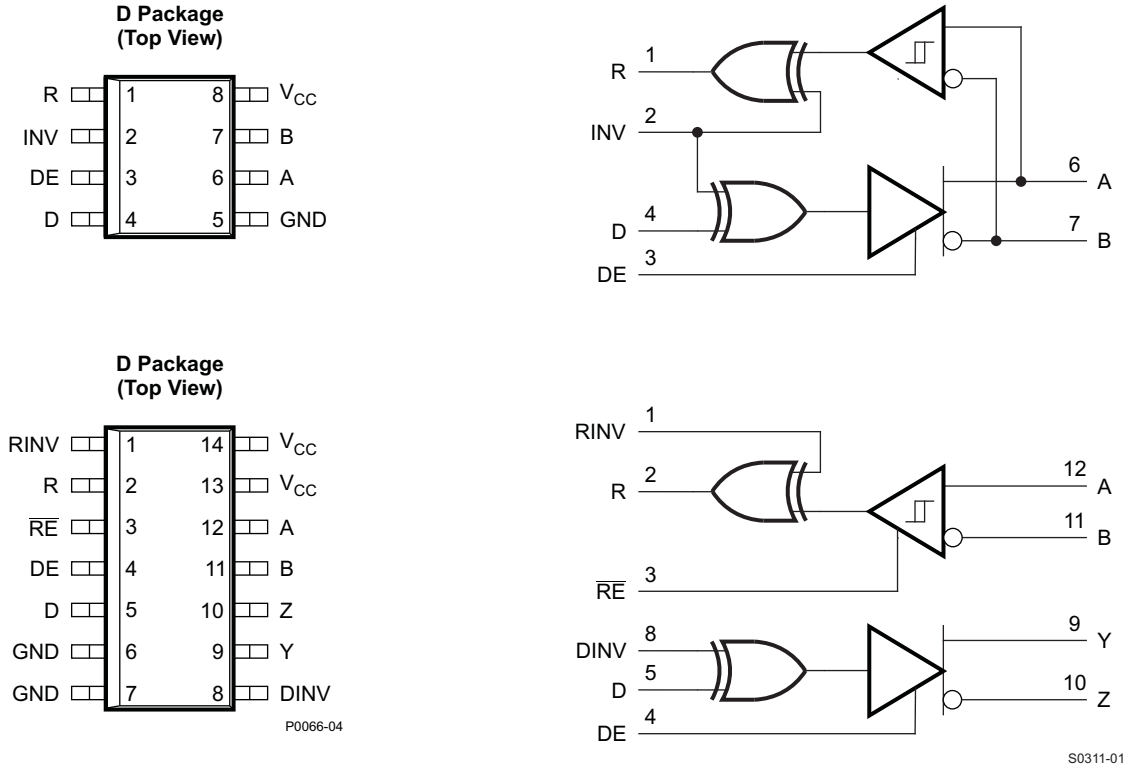


Figure 14. SN65HVD17xx Options With Inverting Feature to Correct for Miswired Cables

APPLICATION INFORMATION

Hot-Plugging

These devices are designed to operate in "hot swap" or "hot pluggable" applications. Key features for hot-pluggable applications are power-up, power-down glitch free operation, default disabled input/output pins, and receiver failsafe. As shown in [Figure 9](#), an internal Power-On Reset circuit keeps the driver outputs in a high-impedance state until the supply voltage has reached a level at which the device will reliably operate. This ensures that no spurious transitions (glitches) will occur on the bus pin outputs as the power supply turns on or turns off.

As shown in the device **FUNCTION TABLE**, the *ENABLE* inputs have the feature of default disable on both the driver enable and receiver enable. This ensures that the device will neither drive the bus nor report data on the R pin until the associated controller actively drives the enable pins.

Likewise, the receiver output is "failsafe" to open-circuit, short-circuit, or idle (terminated only) bus conditions. This eliminates false transitions on the receiver output until a valid RS-485 signal is applied to the receiver input pins.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN65HVD1785D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD1785DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD1785DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD1785DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD1785P	ACTIVE	PDIP	P	8	50	TBD	CU NIPDAU	N / A for Pkg Type
SN65HVD1786D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD1786DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD1786DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD1786DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD1786P	ACTIVE	PDIP	P	8	50	TBD	CU NIPDAU	N / A for Pkg Type
SN65HVD1787D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD1787DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD1787DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD1787DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD1787P	PREVIEW	PDIP	P	8	50	TBD	Call TI	Call TI
SN65HVD1791D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD1791DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD1791DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD1791DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD1792D	PREVIEW	SOIC	D	14	50	TBD	Call TI	Call TI
SN65HVD1792DR	PREVIEW	SOIC	D	14	2500	TBD	Call TI	Call TI
SN65HVD1793D	PREVIEW	SOIC	D	14	50	TBD	Call TI	Call TI
SN65HVD1793DR	PREVIEW	SOIC	D	14	2500	TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

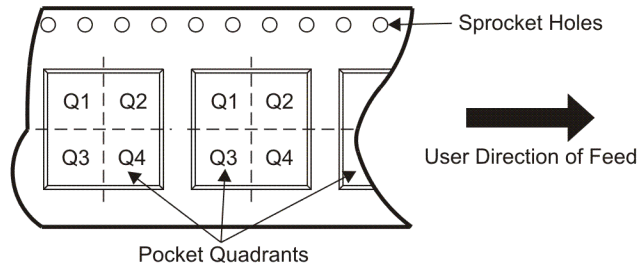
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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD1785DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD1786DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD1787DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD1791DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

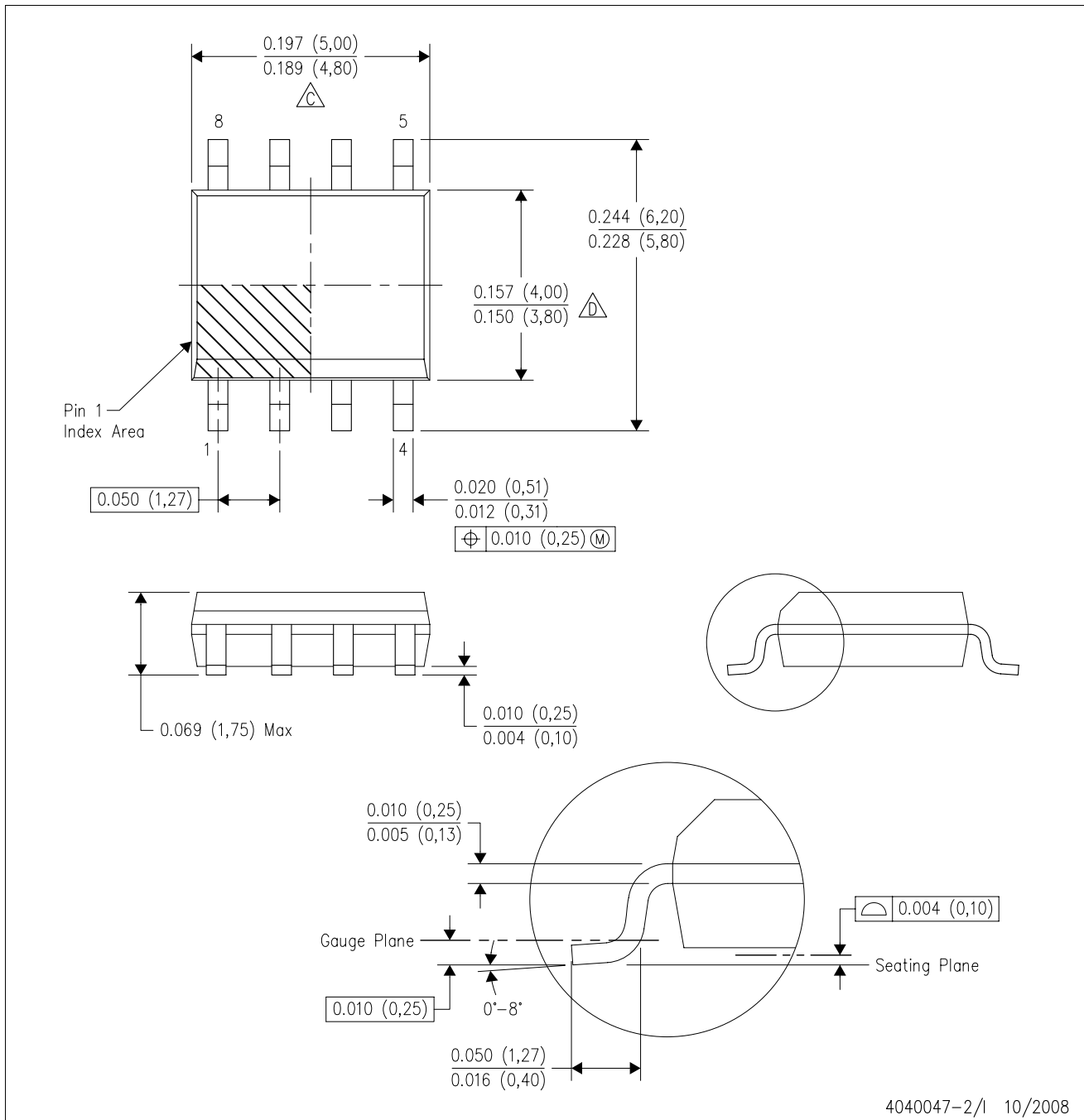


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD1785DR	SOIC	D	8	2500	346.0	346.0	29.0
SN65HVD1786DR	SOIC	D	8	2500	346.0	346.0	29.0
SN65HVD1787DR	SOIC	D	8	2500	346.0	346.0	29.0
SN65HVD1791DR	SOIC	D	14	2500	346.0	346.0	33.0

D (R-PDSO-G8)

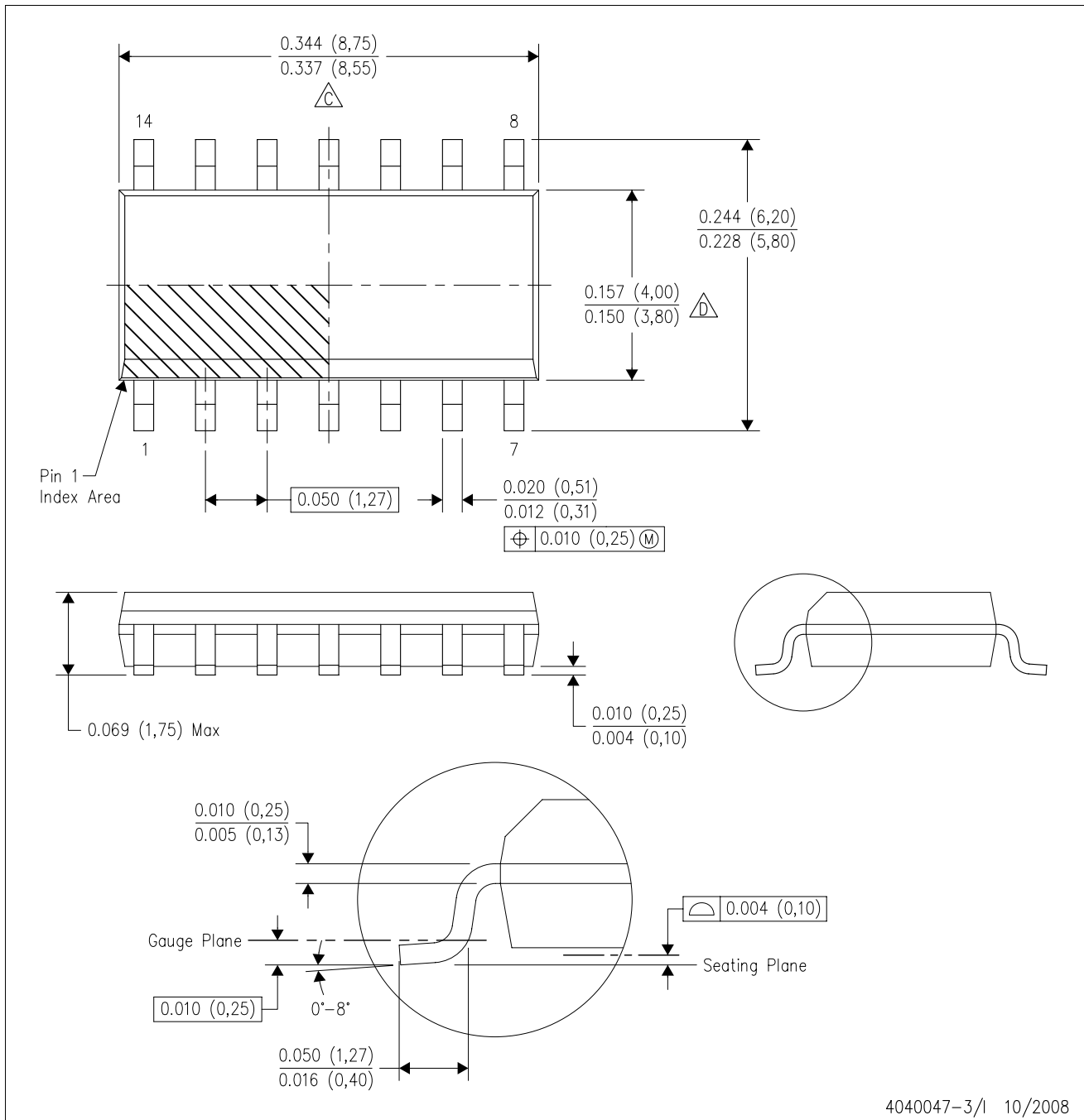
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G14)

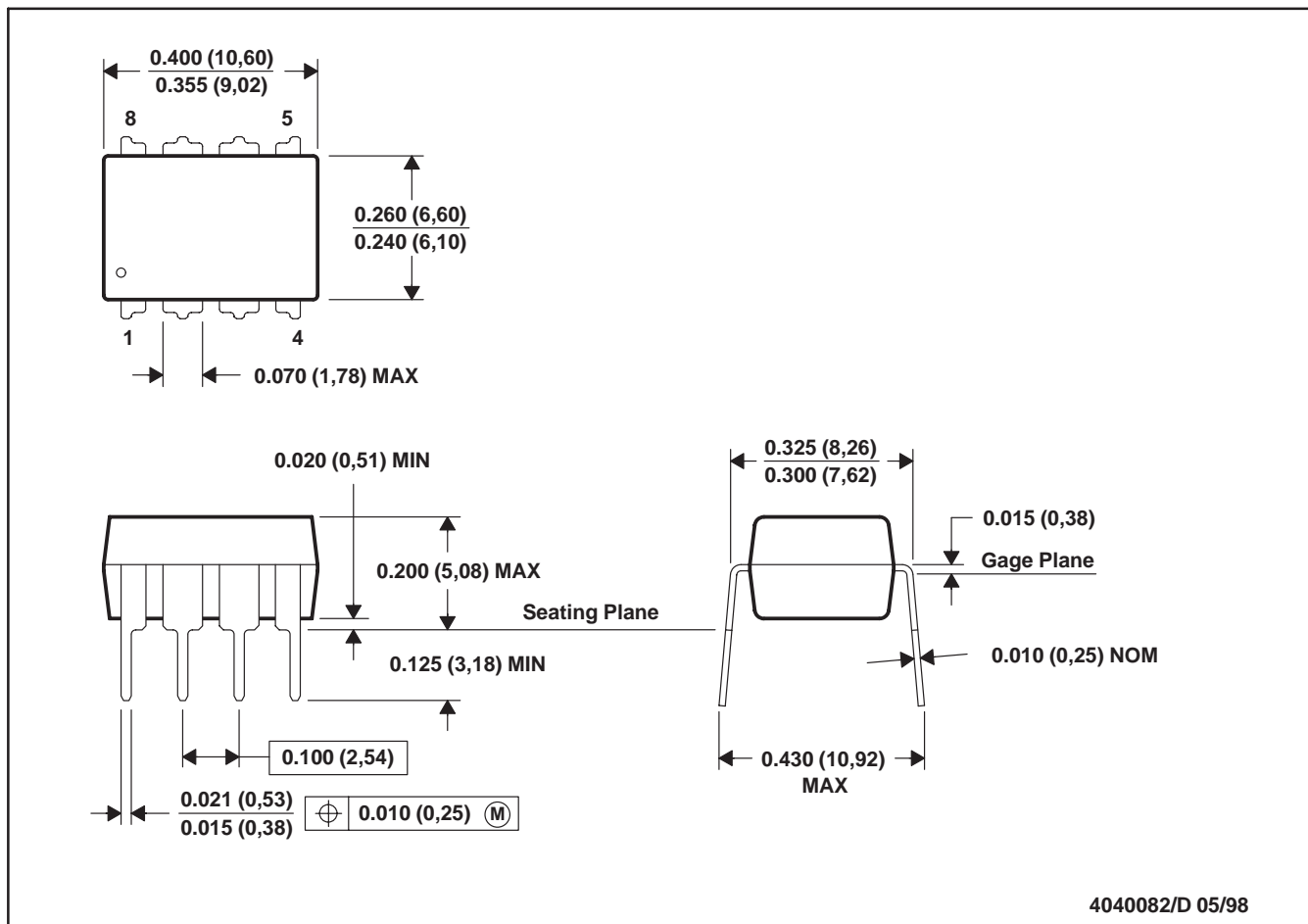
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AB.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-001

For the latest package information, go to http://www.ti.com/sc/docs/package/pkg_info.htm



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